SEMICONDUCTOR CONDUCTIVE PATTERN FORMATION METHOD

RELATED APPLICATIONS

This application claims the benefit of serial number 60/171,259, entitled "Method for Etching Copper," filed provisionally on December 15, 1999.

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to the field of semiconductors, and more particularly to a semiconductor conductive pattern formation method.

BACKGROUND OF THE INVENTION

Ultra-large scale integrated circuits (ULSI), microelectronics, optoelectronics, and other electronic devices and products generally require fine interconnection or conductive patterns to accommodate functionality and density constraints. However, fine interconnection patterns are increasingly difficult to control. For example, one material used to form interconnection patterns is copper. Copper may be used for interconnection patterns rather than aluminum materials because copper generally has a higher conductivity, substantially no hillocks formation, and substantially no electron migration. Actually, copper interconnection may be required for the sub 180 nanometer ULSI. However, one problem associated with copper trace or line formation is that there is a lack of an effective dry etching process to prepare well-controlled copper fine lines. For example, copper lines are generally prepared with a chemical mechanical polishing (CMP) process, such as Damascene or dual-Damascene. However, when the minimum device geometry is reduced or shrunk to less than 100 nanometers, such a process is especially difficult for use in etching and filling high aspect ratio structures.

Plasma etching of copper has also been used to form interconnection patterns. For example, the most common etching chemistry is derived from an aluminum etch, i.e., using halogen-containing gases as the feed streams. Since the reaction products of the plasma etch, i.e., copper halides, have very low volatilities at room temperature, the reaction products often accumulate on

the surface of the product or device instead of being removed. In order to facilitate the removal of these halides, a high-energy source, such as a high-density plasma, a laser, an infrared (IR) or ultraviolet (UV) beam, or a high substrate temperature, needs to be added to a reactive ion etching (RIE) chamber. Such methods either may have poor etch uniformity for large area substrates or require a complicated reactor design and process control scheme. The high temperature approach does not have the above described problems, but still requires high ion bombardment energy to achieve a high etch rate. Additionally, the selectivity of copper or other interconnection materials to another film will generally be lowered by the high ion bombardment energy. In many of the copper etching processes, for example, the etch rate is negative, i.e., the etched surface is higher than the unetched surface due to the accumulation of the reaction product.

SUMMARY OF THE INVENTION

Accordingly, a need has arisen for an improved interconnection or conductive pattern forming method for microelectronic, optoelectronic and other electronic devices. The present invention provides a method for conductive pattern formation that addresses disadvantages and problems associated with previous conductive pattern formation methods.

In accordance with one embodiment of the present invention, a method for forming a conductive pattern for a semiconductor device includes patterning a mask layer outwardly from a conductive layer of the semiconductor device. The patterning defines portions of the conductive layer where vias or open areas through the conductive layer are desired. The method also includes exposing the semiconductor device to a plasma. The plasma converts the unmasked portions of the conductive layer into a compound. The method further includes exposing the semiconductor device to a treatment process to selectively remove the compound.

According to another embodiment of the present invention, a method for forming a conductive pattern for an electronic device includes forming a conductive layer outwardly from a substrate of the electronic device and patterning a mask layer outwardly from the conductive layer. The patterning defines portions of the conductive layer where vias or open areas through the conductive layer are desired. The method also includes exposing the electronic device to a plasma. The plasma converts the unmasked portions of the conductive layer into a compound. The method further includes exposing the

semiconductor device to a treatment process to selectively remove the compound. The method also includes removing the mask layer from the masked portions of the conductive layer.

The present invention provides several technical advantages. For example, the present invention provides conductive pattern formation using a generally high etch rate. Another advantage of the present invention is that the prevention may be applied to a large-area substrate. A further advantage of the present invention is that the method is compatible with other semiconductor processes and device requirements.

Other aspects and technical advantages will be readily apparent to one skilled in the art from the following figures, descriptions and claims.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings, in which:

FIGURE 1 illustrates a schematic cross-sectional diagram of a semiconductor device having a mask layer formed over a conductive layer that is deposited on a substrate in accordance with an embodiment of the present invention;

FIGURE 2 illustrates a schematic cross-sectional diagram of the semiconductor device of FIGURE 1 after plasma exposure in accordance with an embodiment of the present invention;

FIGURE 3 illustrates a schematic cross-sectional diagram of the semiconductor device of FIGURES 1 and 2 after plasma-converted compound layer material removal in accordance with an embodiment of the present invention;

FIGURE 4 illustrates a schematic cross-sectional diagram of the semiconductor device of FIGURES 1-3 after the mask layer and the compound removal in accordance with an embodiment of the present invention; and

FIGURE 5 is a flow diagram illustrating conductive pattern formation in accordance with an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

FIGURES 1-4 illustrate the formation of an electronic device 10 in accordance with an embodiment of the present invention. Device 10 may include a semiconductor device, microelectronic device, optoelectronic device, magnetic device, or any other device requiring a conductive interconnection pattern.

Referring to FIGURE 1, a conductive layer 12 and a barrier layer 14 are formed upwardly from a substrate 16. Substrate 16 may include glass, silicon, plastic, metal, or any other suitable substrate material. Barrier layer 14 may include titanium, titanium oxide, titanium nitride, tantalum, tantalum oxide, tantalum nitride, chromium, or any other suitable material to enhance the adhesion of the conductive layer 12 and/or to substantially prevent diffusion of the material comprising the conductive layer 12 into the substrate 16. Thus, layer 14 may comprise either conductive or non-conductive materials corresponding to a particular application. However, it should be understood that conductive layer 12 may also be formed upwardly from substrate 16 without barrier layer 14.

Conductive layer 12 may include copper, nickel, and iron, alloys or compounds of copper, nickel and iron, or other suitable conductive materials for providing conductive interconnections or magnetic patterns on the device 10. As illustrated in FIGURE 1, one or more mask layers 18 are formed upwardly from conductive layer 12 to define open areas or vias 20 through the conductive layer 12 at desired locations. For example, one or more of the mask layers 18 are formed over the conductive layer 12 to

define a desired conductive or magnetic pattern for the device 10, thereby masking a portion of the conductive layer 12 that will remain on the device 10. Unmasked portions of the conductive layer 12 corresponding to the vias 20 are removed, as will be discussed in greater detail below, thereby forming open areas or vias 20 through the conductive layer 12.

In the embodiment illustrated in FIGURE 1, mask layers 18 include a hard masking layer 22 formed upwardly from the conductive layer 12, and a photoresist layer 24 formed upwardly from the masking layer 22. The function of layer 22 is to provide a protection, a passivation, or a diffusion barrier to the conductive layer 12. Masking layer 22 may include silicon oxide, silicon nitride, metals, metal oxides, or other suitable materials to provide additional etching layers of device 10 to accommodate a variety of pattern formations and/or etching techniques. However, it should be understood that photoresist layer 24 may be formed upwardly from the conductive layer 12 without the masking layer 22.

Referring to FIGURE 2, device 10 is then exposed to a plasma in a plasma reactor (not explicitly shown). The plasma reactor may have a conventional simple parallel-plate design or have a high density plasma (such as inductive-coupled plasma ICP, electron cyclotron resonance ECR, hellicon plasma, or other suitable designs). The plasma exposure may be performed using conventional plasma etching or deposition techniques, such as, but not limited to, 1 mTorr to 10 Torr pressure. An electrode, located generally where device 10 is loaded into the reactor, may be heated with an electric heater,

a hot oil coil, an infrared source, or other suitable methods. A wide range of substrate 10 temperatures may be used during the plasma exposure, such as, but not limited to, from lower than room temperature to approximately 500 degrees Celsius.

The plasma includes one of a variety of gases comprising an element selected from the halogen group of elements, such as, but not limited to, chlorine, bromine, fluorine, iodine, or their mixtures, as the reactive component in the feed stream of the plasma exposure process. For example, the plasma may include a chlorine-containing gas such as HCl, Cl_2, organic or inorganic chloride, HBr, Br_2, HI, I_2 or their mixtures. Other gases, such as, but not limited to, oxygen, inert gases, and nitrogen may be mixed with the reactive component to enhance the plasma-conductive layer 12 reaction.

Referring to FIGURE 2, a cross-sectional view of device 10 is illustrated after the plasma exposure. As illustrated in FIGURE 2, unmasked portions of the conductive layer 12 are converted into a compound layer 30 as a result of the chemical reaction between the plasma and the exposed portions of the conductive layer 12. For example, if the conductive layer 12 comprises copper and the plasma comprises an HCl plasma, a copper chloride layer may be formed as compound layer 30.

Depending on the reaction mechanism and process characteristics, the compound layer 30 may be thicker than the original conductive layer 12. For example, the compound layer 30 may grow isotropically when it is higher than the mask layers 18. Additionally, the plasma exposure process may also be controlled to for form an

interface between the masked portion of the conductive layer 12 and the compound layer 30 that is substantially perpendicular to the surface of the substrate 16. The plasma exposure process may also be controlled to form a sloped or angled interface at a variety of angular orientations between the masked portion of the layer 12 and the compound layer 30. Such plasma exposure characteristics as the gas type, pressure, power, time, and the substrate temperature may be varied to form a desired interface between the masked portion of the conductive layer 12 and the compound layer 30.

Referring to FIGURE 3, the device 10 is illustrated after removal of the compound layer 30. The device 10 may be exposed to a physical or chemical environment or process to remove the compound layer 30. For example, if the compound layer 30 comprises copper chloride resulting from the reaction of a copper material conductive layer 12 with a HCl plasma as described above, a hydrogen chloride (HCl) solution may be used to remove the compound layer 30 with substantially little affect to the remaining conductive layer 12 and/or mask layers 18. In another method, using copper chloride as the compound layer 30 for example, the copper chloride may be removed by heating the device 10 to a high temperature, such as between 500-600 degrees Celsius, under vacuum or in an inert atmosphere because the copper chloride material has generally a much lower higher vapor pressure than copper material. Another alternative method includes exposing the device 10 to an energized electron or ion beam that will evaporate the compound layer 30. A laser, IR, or UV beam could also be used to remove the compound layer 30.

However, other suitable methods or techniques may also be used to remove the compound layer 30.

Referring to FIGURE 4, the device 10 is illustrated after removal of portions of layer 14 corresponding to the vias 20 and the mask layers 18, thereby providing the desired conductive or magnetic pattern. Layer 14 may be selectively removed from the via 20 locations using conventional methods, including, but not limited to, etching processes. However, it should be understood that layer 14 may remain on the device 10, for example, if layer 14 comprises an insulating material. The mask layers 18 may be removed using conventional methods such as, but not limited to, a plasma process, a solvent dipping, or a combination of plasma processes and solvent dipping. For example, the photoresist layer 24 may be removed using an acetone solution in an ultrasonic bath at approximately sixty degrees Celsius. However, other suitable methods may also be used to remove the mask layers 18. Additionally, the mask layers 18 may be removed either before or after the removal of the compound layer 30, and layer 14 may be removed either after or before removal of the mask layers 18.

FIGURE 5 is a flow diagram illustrating a method for conductive pattern formation on a device 10 in accordance with an embodiment of the present invention. The method begins at step 100, where the barrier layer 14 is formed upwardly from the substrate 16. However, it should be understood that the barrier layer 14 may be omitted to accommodate a particular device 10 configuration or materials selection. At step 102, conductive layer 12 is formed upwardly from barrier layer 14, or upwardly from

the substrate 16 if the barrier layer 14 was omitted. As described above, the conductive layer 12 may include copper, nickel, iron, or other suitable conductive or magnetic materials.

At step 104, one or more mask layers 18 are formed upwardly over portions of the conductive layer 12 to define a desired conductive pattern. For example, a mask layer 18 is configured to a desired conductive pattern for the device 10, thereby creating vias 20 corresponding to unmasked portions of the conductive layer 12 that will be removed to form the desired conductive pattern. At step 106, the device is exposed to a plasma in a plasma reactor. As described above, the plasma comprises a gas selected from the halogen group of elements such as, but not limited to, chlorine, bromine, fluorine, and iodine. At step 108, exposure of the device 10 to the plasma converts the unmasked portions of the conductive layer 12 to a compound layer 30.

At decisional step 110, a determination is made whether to remove the mask layers 18 before or after removal of the compound layer 30. If removal of the mask layers 18 is desired before removing the compound layer 30, the method proceeds to step 112, where mask layers 18 are removed using conventional methods. If removal of the mask layers 18 is desired after removal of the compound layer 30, the method proceeds from step 110 to step 114.

At step 114, the compound layer 30 is removed from the device 10, thereby forming the open areas or vias 20 in the conductive layer 12 corresponding to the previously unmasked portions of the conductive layer 12.

At step 115, layer 14 may be removed from the substrate 16 corresponding to the via 20 locations. As described above, layer 14 may be removed either after or before removal of the mask layers 18. At decisional step 116, a determination is made whether the mask layers 18 were previously removed. If the mask layers 18 were not removed before removal of the compound layer 30, the method proceeds from step 116 to step 118, where the mask layers 18 are removed. If the mask layers 18 were removed prior to removal of the compound layer 30, the method terminates.

Thus, the present invention provides a conductive pattern formation method that provides greater control and creation of fine conductive interconnection lines or traces for semiconductors and other electronic devices than prior conductive pattern formation processes. Additionally, the conductive pattern formation method of the present invention may be used with conventional semiconductor fabrication equipment and facilities, thereby substantially reducing or eliminating costly facility upgrades, retrofits, or the design and manufacturing of unconventional new tools to form fine line conductive or magnetic patterns.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions, and alterations can be made therein without departing from the spirit and scope of the present invention as defined by the appended claims.